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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/655,390	09/04/2003	Gene W. Chen	5500-97900	6653

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EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/655,390	CHEN ET AL.
	Examiner	Art Unit
	Sun J. Lin	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09/04/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/655,390 filed on 09/04/2003.

Claims 1 – 21 remain pending in the application.

Claim Objections

2. Claims listed below are objected to because of the following informalities:

Claim 1, line 5, before "base-level" insert —**plurality of**—.
Claim 2, line 4, before "energy" delete —**an**—.
Claim 8, line 5, before "base-level" insert —**plurality of**—.
Claim 9, line 5, before "energy" delete —**an**—.
Claim 15, line 6, before "base-level" insert —**plurality of**—.
Claim 16, line 5, before "energy" delete —**an**—.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1 – 3, 5 – 7, 8 – 10, 12 – 14, 15 – 17 and 19 – 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over IEEE paper entitled " *Evaluation of Architectural-level Power Estimation for CMOS RISC Processors*" authored by Sato *et*

al. in view of IEEE paper entitled "*Analytical Energy dissipation Models for Low power Caches*" authored by *Kamble et al.*

5. As to Claim 1, *Sato et al.* disclose the following subject matter:

- Architectural power estimation for CMOS RISC processors, ESP (Early design Stage Power and performance simulator – [title; abstract]; Notice that (1) power dissipation of a CMOS RISC processor is a energy event (2) *power estimation* is performed based on a *power model*
- Base-level power estimation for each of *basic components*, namely *control, datapath and cache*, of a CMOS RISC processor – [ESP and VeriPower]; Notice that a base-level power model is generated to estimate power consumption of each (basic) component of the CMOS RISC processor.

et al. Sato et al. disclose using ESP to estimate power consumption of each active component at each clock cycle – [ESP and VeriPower]. They do not explicitly disclose relationship between a power model and an energy model associated with a basic component of the CMOS RISC processor. *Kamble et al.* teach using energy (dissipation) models for analyzing power consumption in design of low power caches – [title, abstract, pp143]. *Kamble et al.* teach using a power estimation model to instantiates a set of base-level energy models for constituent components (e.g., bit lines, word lines, output lines, address input lines etc.) of a cache in order to accurately estimate total energy/power consumption of an energy event in design a low power cache. Notice that the teachings of *Kamble et al.* can be in modeling and analyzing power/energy of caches in different hierarchy.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Kamble et al.* in using a power estimation model to hierarchically instantiates a set of base-level energy models for constituent components (e.g., bit lines, word lines, output lines, address input lines etc.) of a cache in order to accurately estimate total energy/power consumption of an energy event in design a low power cache included in a CMOS RISC processor.

It is well known in the art that mapping each energy event to a set of power models is to estimate power consumption in order to design a device having low energy consumption.

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

6. As to Claims 8 and 15, reasons are included in **[Response A]** given above.

7. As to Claims 2, 9 and 16, reasons regarding hierarchically evaluating and estimating energy are included in **[Response A]** given above. *Kamble et al.* teach accumulating energy (consumption) in a power estimate corresponding to a cache in a energy event associated with CMOS RISC processor – [Equation 9; Response A].

8. As to Claims 3, 5, 10, 12, 17 and 19, *Kamble et al.* show and teach the subject matter in Section 2 – [Equations 1 – 9; pp. 143 – 145].

9. As to Claims 6, 13 and 20, *Sato et al.* show in Fig. 3 and teach that energy of a datapath is estimated and scaled based on *input vectors* (i.e., *input data pattern*) to each component. Notice that the *input vectors* (*input data pattern*) are *data value parameters*.

10. As to Claims 7, 14 and 21, *base-level energy models* are energy models of a set of functional building blocks, they can be stored in a library for use in future retrieval or upgrades/modifications.

11. Claims 4, 11 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over IEEE paper entitled " *Evaluation of Architectural-level Power Estimation for CMOS RISC Processors*" authored by *Sato et al.* and IEEE paper entitled "*Analytical Energy dissipation Models for Low power Caches*" authored by *Kamble et al.* in view of IEEE paper entitled " Impact of Technology Scaling in the Clock System Power" authored by *Duarte et al.*

12. As to Claim 4, *Sato et al.* and *Kamble et al.* teach all subject matter recited in Claim 3, they do not teach using an *aspect ratio parameter* for scaling an energy estimate for energy modeling of a basic function component. But *Duarte et al.* teach utilization of scaling parameters in predicting clock power consumption in various architecture and physical sizes due to different technologies – [Section 3].

Notice that the aspect ratio parameter is included in the energy (estimation) model in order to scale energy estimate thereby accurately predict energy consumption of a basic component manufactured in different technologies.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Duarte et al.* in including aspect ratio parameter in the energy (estimation) model in order to scale energy estimate thereby accurately predict energy consumption of a basic component manufactured in different technologies.

For reference purposes, the explanations given above in response to Claim 4 are called **[Response B]** hereinafter.

13. As to Claims 11 and 18, reasons are included in **[Response B]** given above.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Patent Examiner
Art Unit 2825
September 17, 2005